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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/669,852

09/25/2003

Toshiyuki Kasai

117024

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05/17/2006

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EXAMINER

GOKHALE, SAMEER K

ART UNIT

PAPER NUMBER

2629

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/669,852	<b>Applicant(s)</b> KASAI, TOSHIYUKI	
	<b>Examiner</b> Sameer K. Gokhale	<b>Art Unit</b> 2629	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 April 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9, 11-22 and 24-28 is/are rejected.
- 7) ☒ Claim(s) 10 and 23 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                                                                   |                                                                                         |
|-----------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                                       | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                              | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 9, 11-22, and 24-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Kimura (US 6,909,242).

Regarding claims 1-5, and 14-18, Kimura teaches an electronic circuit and an electronic device (Fig. 33A), comprising:

a first signal line (Fig. 33A, line 3302), a second signal line (Fig. 33A, line 3301, and a plurality of unit circuits (Fig. 33A), each of the plurality of unit circuits comprising:

a switching element connected to the first signal line (Fig. 33A, switch 3306), an on/off state of the switching element being controlled by switching signals supplied from the first signal line (col. 38, lines 51-52);

a first circuit unit connected to the second signal line (Fig. 33C, the first circuit being the circuit involved in sending the current along the shown path), a first current (Fig. 33C, I<sub>data</sub>) having a first current level supplied from the second signal line (Fig.

33C, Idata is supplied from line 3301) passing through the first circuit unit by switching on the switching element (Fig. 33C, switch 3306 is 'ON');

a capacitor element (Fig. 33A, capacitor 3312) to store a quantity of electric charge corresponding to the first current level (Fig. 33C); and

a second circuit unit (Fig. 33D, the second circuit being the circuit involved in sending the current along the shown path) to generate a second current (Fig. 33D, current IEL) having a second current level different from the first current level on the basis of the quantity of electric charge stored in the capacitor element (col. 40, lines 7-23),

the first circuit unit including a plurality of unit elements connected in parallel (Fig. 33B, switch 3309 and capacitor 3312 are connected in parallel for the first circuit),

the second circuit unit including a plurality of unit elements connected in series (Fig. 33D, switch 3310 and switch 3309 are connected in series for the second circuit),

the electrical connections of the plurality of unit elements being controlled by a control element (Fig. 3A, gate driver 304, see col. 21, lines 9-12, where the gate driver controls the signals sent to the source signal lines that control the electrical connections of the switches described above).

Regarding claims 6 and 19, Kimura teaches an electronic circuit and device where at least one of the plurality of unit elements being a unit element common to the first circuit unit and the second circuit unit (Figs. 33A-33D, where either capacitor 3312 or switch 3309 fulfills this role).

Regarding claims 7 and 20, Kimura teaches an electronic circuit and device where the plurality of unit elements have the same driving capability (see col. 7, lines 46-48, where the TFT elements can be “common” or the same).

Regarding claims 8 and 21, Kimura teaches an electronic circuit and device where the plurality of unit elements are formed in a bundle (Fig. 33A, where the unit elements here are considered “bundled” since they are close together).

Regarding claims 9 and 22, Kimura teaches an electronic circuit and device where the first current level is higher than the second current level (see col. 40, lines 35-36, where  $I_{data}$  is greater than  $I_{EL}$ ).

Regarding claims 11 and 24, Kimura teaches an electronic circuit and device where there are electronic elements being supplied with the second current (Fig. 33D, where element 3313 is supplied with the second current,  $I_{EL}$ ).

Regarding claims 12 and 25, Kimura teaches an electronic circuit and device where the electronic elements is an electro-optical element or a current-driven element (col. 38, lines 49-50, where an EL element is an electro-optical element).

Regarding claims 13 and 26, Kimura teaches an electronic circuit and device where the electronic element is an organic EL element (col. 38, lines 49-50, and col. 31, line 44).

Regarding claims 27 and 28, Kimura teaches an electronic apparatus having mounted therein the electronic circuit and device (Figs. 16A-16H are all devices that have the circuit and device mounted on it).

### ***Allowable Subject Matter***

3. Claims 10 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Relative to dependent claims 10 and 23, the major difference between the prior art of record (Kimura) and the instant invention is that the said prior art does not teach the second current level being higher than the first current level.

### ***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Koyama (US 6,876,350) teaches an EL display device that features elements in parallel and in series. Yamagishi et al. (US 6,501,466) teaches an

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active matrix display with elements in parallel and in series. Komiya (US 6,924,602) teaches an organic pixel EL circuit with elements in parallel and in series. Shimoda (US 6,809,706) teaches a display device that prevents a decrease in the aperture ratio.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sameer K. Gokhale whose telephone number is (571) 272-5553. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKG  
May 15, 2006

Sameer Gokhale  
Examiner  
Art Unit 2629

AMR A. AWAD  
PRIMARY EXAMINER

